

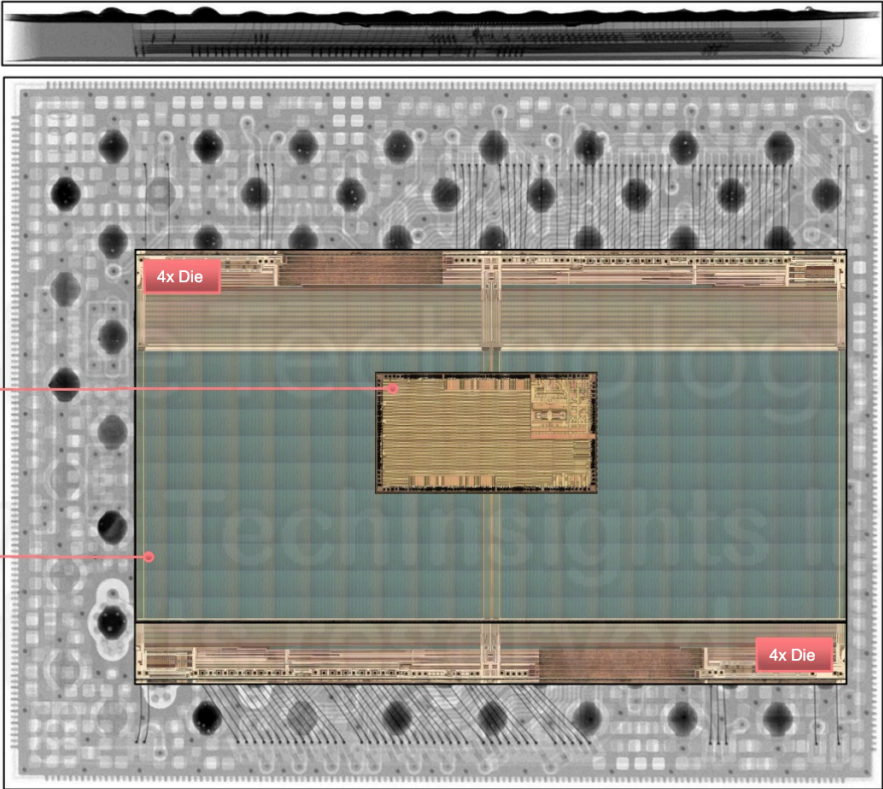
EXHIBIT A

U.S. Patent No. 6,724,241 (“’241 Patent”)

Kioxia products with SanDisk/Toshiba 64L 3D NAND flash chips, including without limitation the Kioxia TSB3245 (“Accused Products”), infringe at least Claims 1-3, 6-8, and 11 of the ’241 Patent. While the infringing structure and functionality of the Accused Products is illustrated below using the Kioxia TSB3245 as an example, all Accused Products operate in substantially the same way for purposes of infringement.

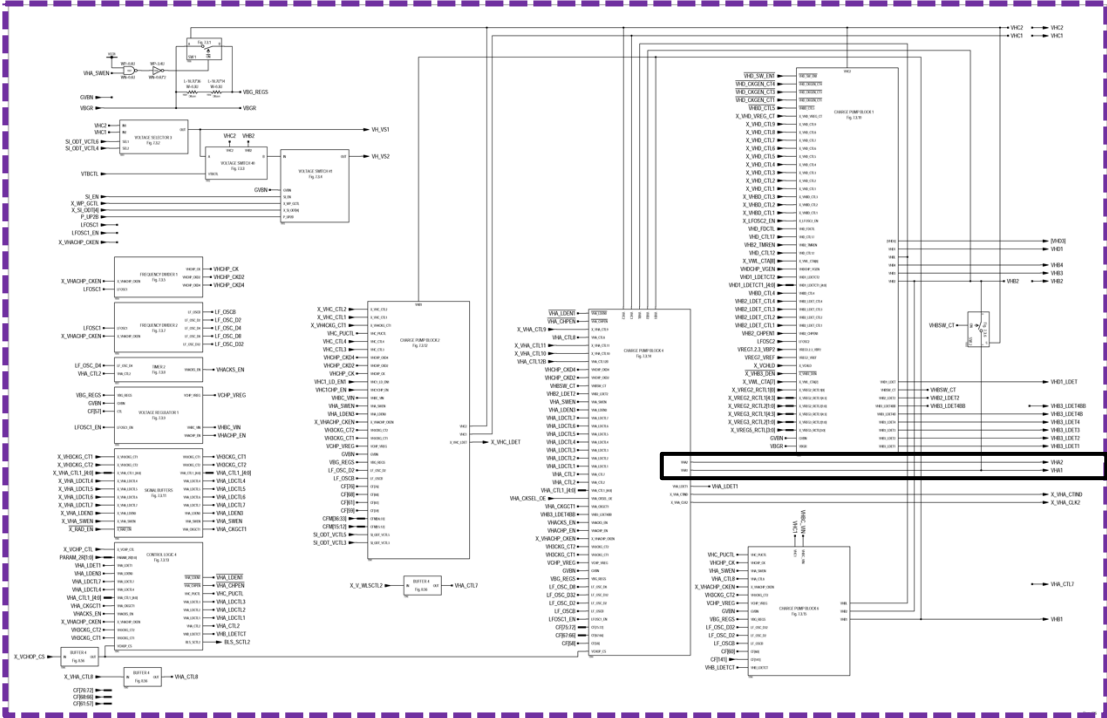
Claim 1

Claim 1	Accused Products
[1pre] 1. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:	<p>To the extent the preamble is limiting, each Accused Product includes a charge pump circuit for generating a charge pump voltage having minimal voltage ripples.</p> <p>For example, the Kioxia TSB3245 includes the charge pump circuit of the SanDisk/Toshiba 3D NAND flash chip, die identifier FRN1256G.</p> <p><i>See, e.g.:</i></p>

Claim 1	Accused Products
	<div data-bbox="655 279 963 370"><p>34 - KIOXIA #TSB3245 Multichip Memory - 256 GB 3D TLC NAND Flash, Memory Controller (9-Die Pkg.) Pkg Size: 14.63 x 11.8 mm</p></div> <div data-bbox="655 626 837 703"><p>34.1 - KIOXIA #TMHM01 Memory Controller Die Size: 3.8 x 2.08 mm</p></div> <div data-bbox="655 794 926 870"><p>34.2 - KIOXIA #FRN1256G 3D TLC NAND Flash Memory - 32 GB Die Size: 12.17 x 6.27 mm</p></div> <div data-bbox="655 1045 835 1086"><p>Function: Memory: Non-Volatile</p></div> <div data-bbox="991 279 1869 1063"></div> <div data-bbox="634 1099 1516 1133"><p>Source: TechInsights Deep Dive Teardown, Apple iPhone SE A2275</p></div>

Claim 1

Accused Products

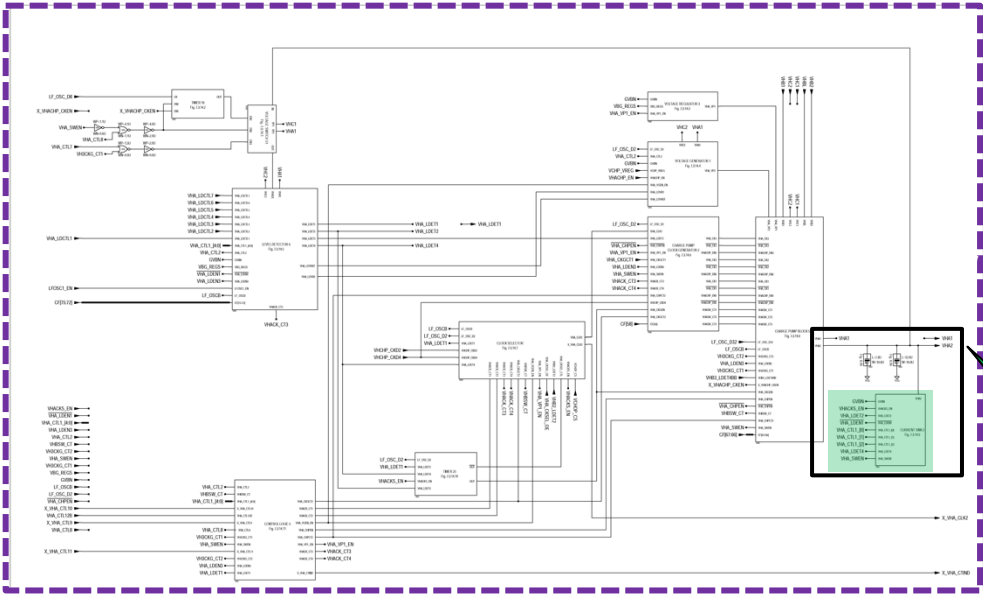


A charge pump circuit

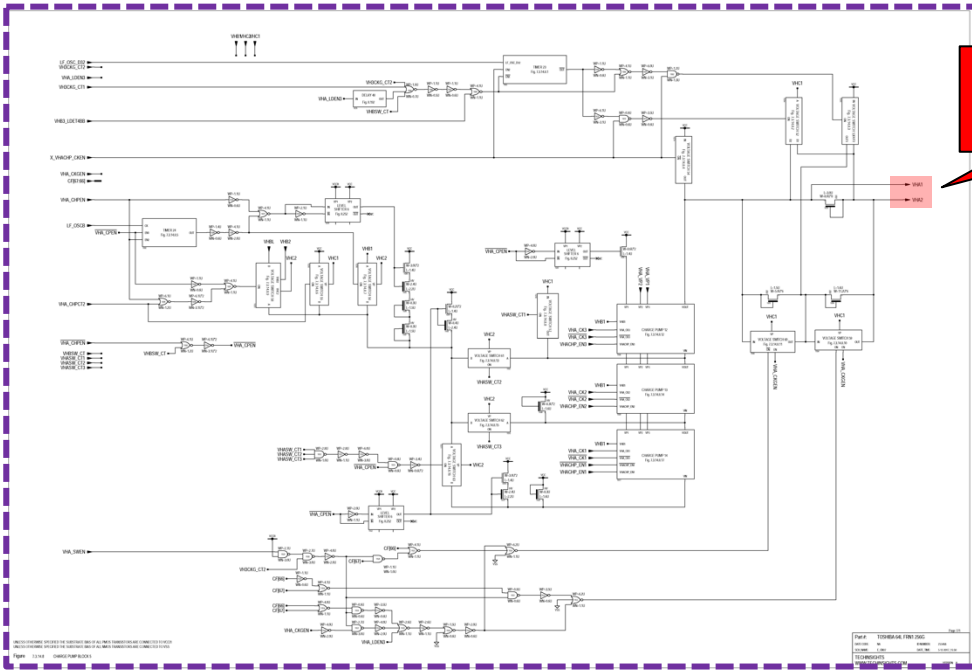
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System

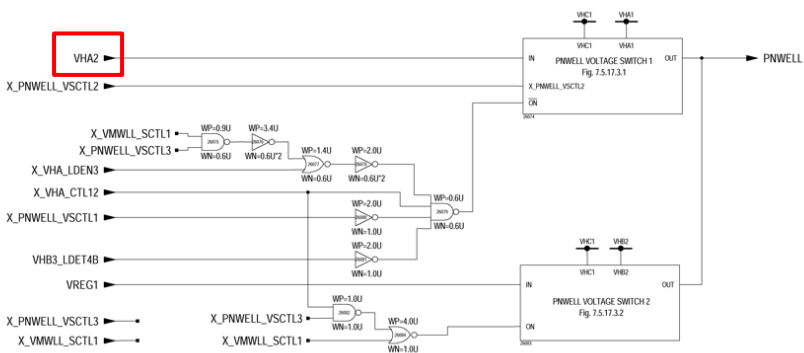
Claim 1

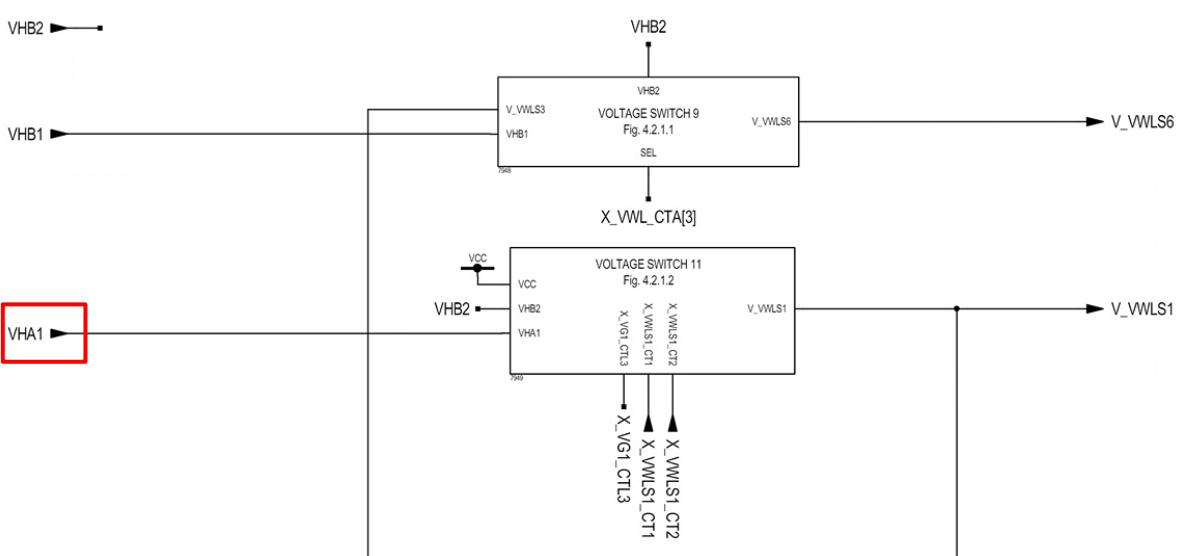
Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System

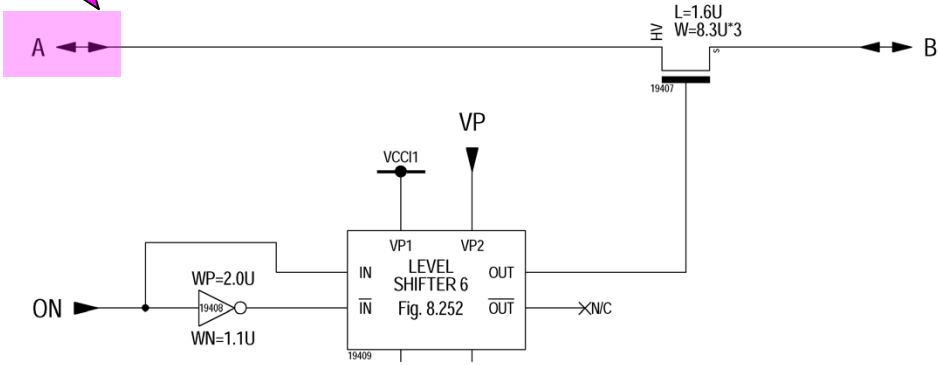
Claim 1	Accused Products
	<div data-bbox="640 267 1606 933"></div> <div data-bbox="1591 310 1871 418" style="background-color: red; color: black; padding: 5px;"><p>for generating a charge pump voltage (VHA1, VHA2)</p></div> <div data-bbox="1612 483 1850 581" style="background-color: white; color: black; padding: 5px;"><p>VHA1 and VHA2 are driven by the same pumping circuit</p></div> <div data-bbox="1625 651 1839 716" style="background-color: purple; color: white; padding: 5px;"><p>A charge pump circuit</p></div>
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5	

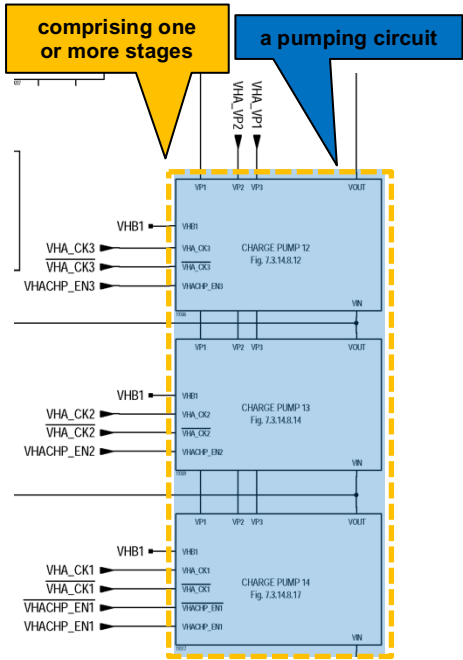
Claim 1	Accused Products
	<p data-bbox="674 300 1241 362">Charge pump output voltage VHA2 is provided to high voltage switches to selectively drive PNWELL.</p>  <p data-bbox="632 829 1829 901">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.5.17.3 PNWELL Voltage Selector</p>

Claim 1	Accused Products
	<p>Charge pump output voltage VHA1 is provided to high voltage switches to selectively drive wordline circuits.</p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>[1a] a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;</p>	<p>Each Accused Product includes a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.</p> <p>For example, in the pumping circuit of the Kioxia TSB3245, 1, 2, or 3 main stages can be enabled for operation. Supply voltage can be selected from external VCC or internally generated pumped voltages VHBL or VHB1. VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage</p>

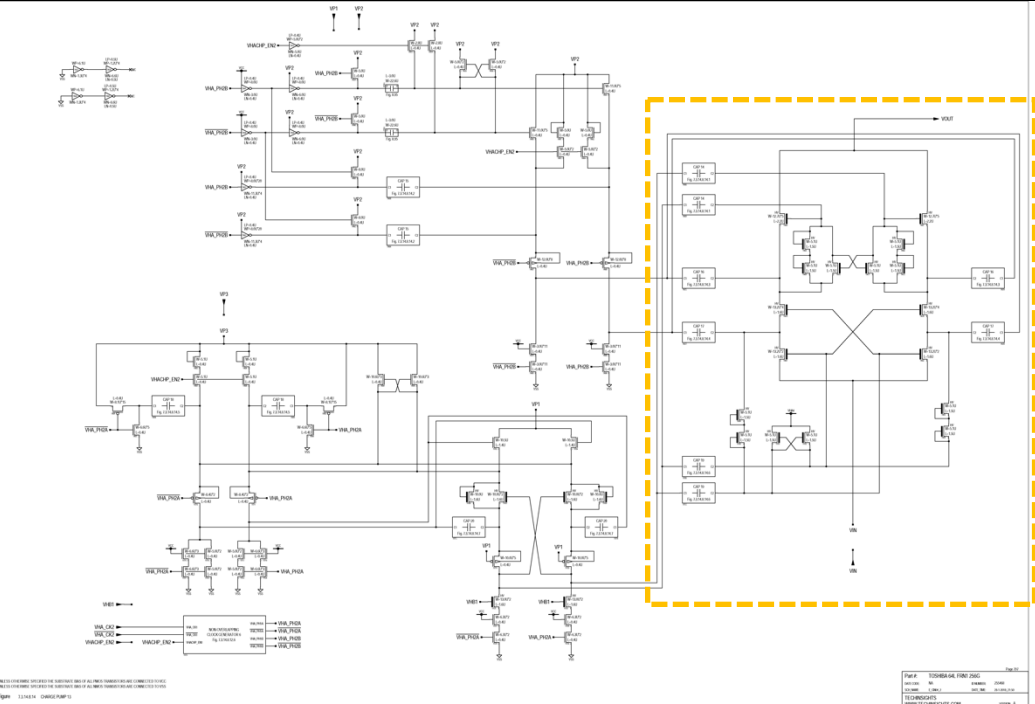
Claim 1	Accused Products
	<p>by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping. VHA_CK2 and VHA_CK2* drive the middle stage of the pumping circuit. VHA_PH2 non-overlapping clocks drive Charge Pump 13. When VHA_PH2 clocks are suspended the pump stops operating so that VHA1 is limited to the voltage set by the level detector.</p> <p><i>See, e.g.:</i></p>

[illegible]

Claim 1	Accused Products
	<p data-bbox="632 266 963 326">operable to receive a supply voltage (VCC)</p>  <p data-bbox="632 792 1829 867">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.6 Voltage Switch 55</p>

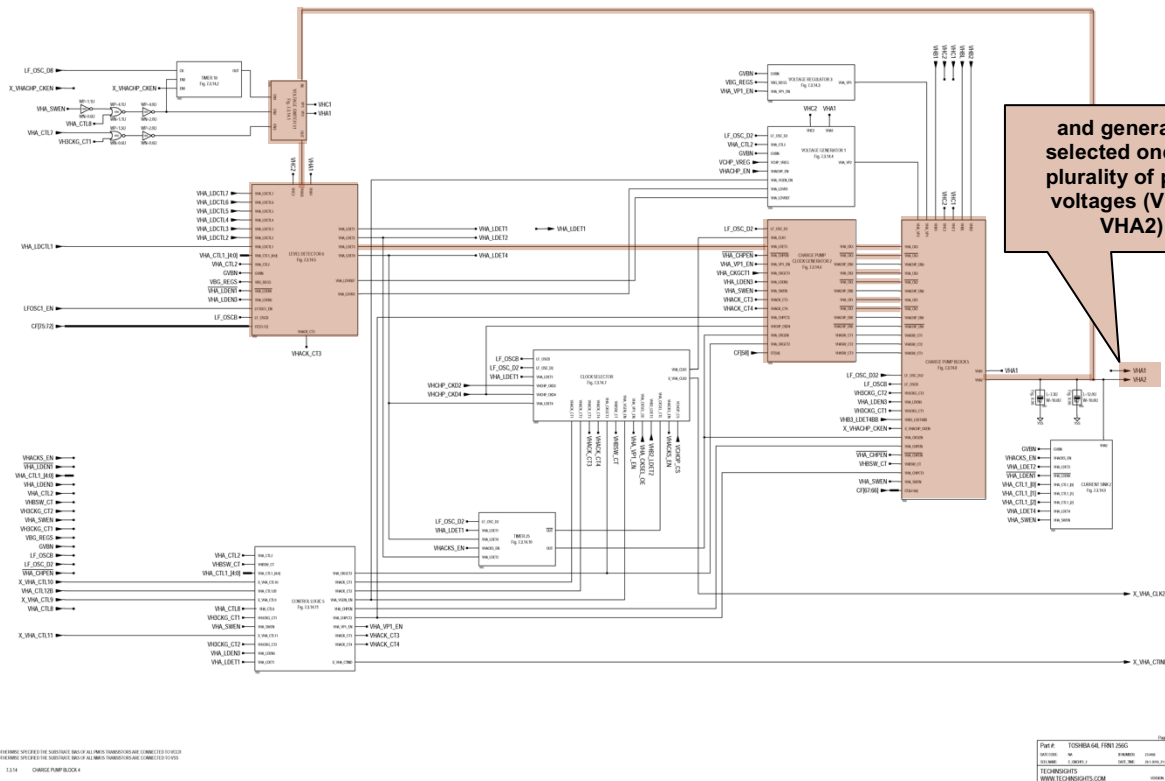
Claim 1	Accused Products
	 <p>The diagram illustrates a multi-stage charge pump circuit, labeled 'Charge Pump Block 5'. It consists of three vertically stacked charge pump stages, each enclosed in a dashed yellow box. The top stage is 'CHARGE PUMP 12' (Fig. 7.3.14.8.12), the middle is 'CHARGE PUMP 13' (Fig. 7.3.14.8.14), and the bottom is 'CHARGE PUMP 14' (Fig. 7.3.14.8.17). Each stage has a common input 'VHB1' and a common output 'VOUT'. The stages are interconnected via 'VHA_CK1', 'VHA_CK2', and 'VHA_CK3' signals. The top stage also receives 'VHA_OK1', 'VHA_OK2', and 'VHA_OK3' signals. The bottom stage receives 'VHA_CHP_EN1', 'VHA_CHP_EN2', and 'VHA_CHP_EN3' signals. A callout 'comprising one or more stages' points to the top stage, and a callout 'a pumping circuit' points to the top stage's output.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

<p>Claim 1</p>	<p>Accused Products</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

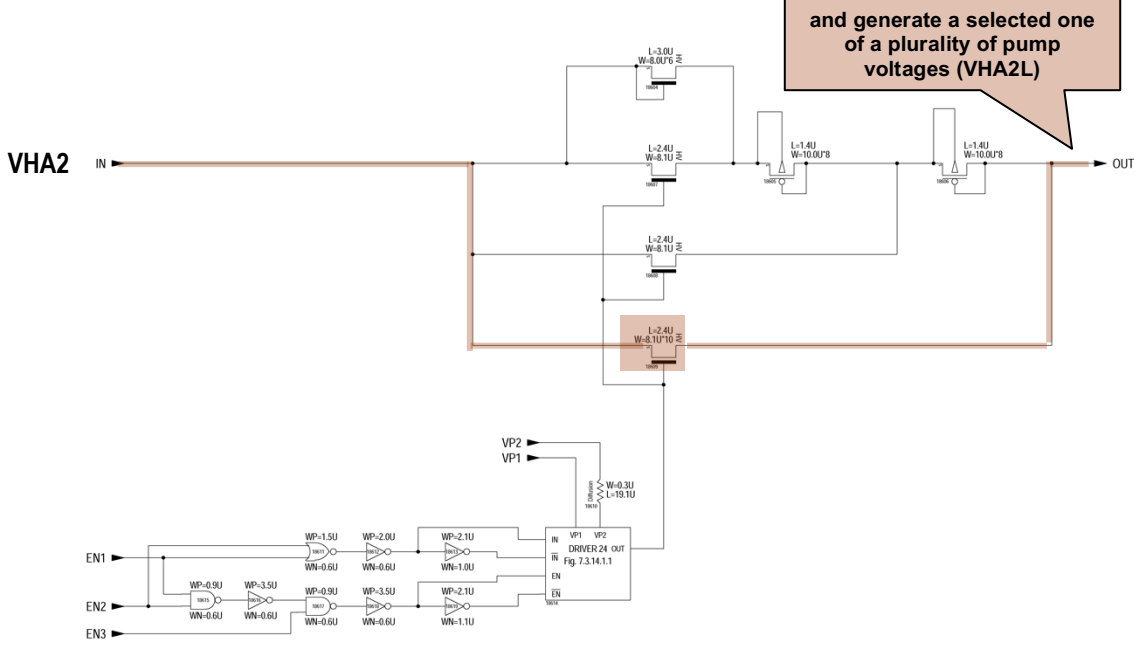
Claim 1	Accused Products
	 <p data-bbox="1680 633 1869 730">comprising one or more stages</p> <p data-bbox="630 990 1827 1055">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

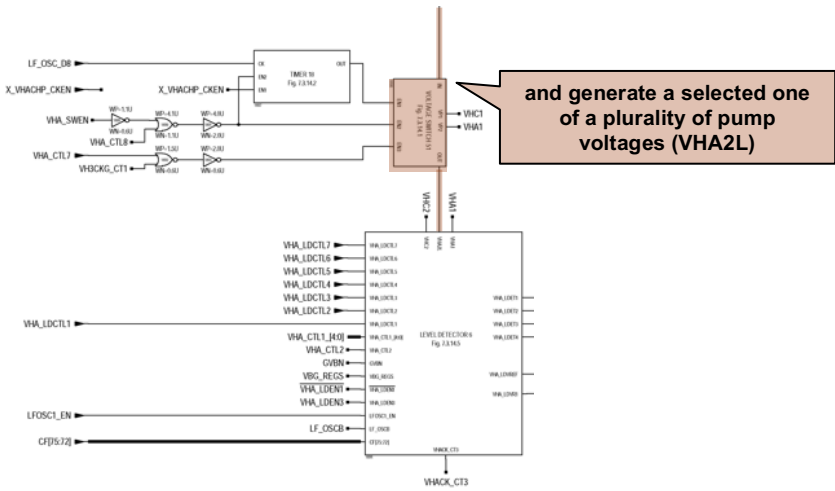
Claim 1

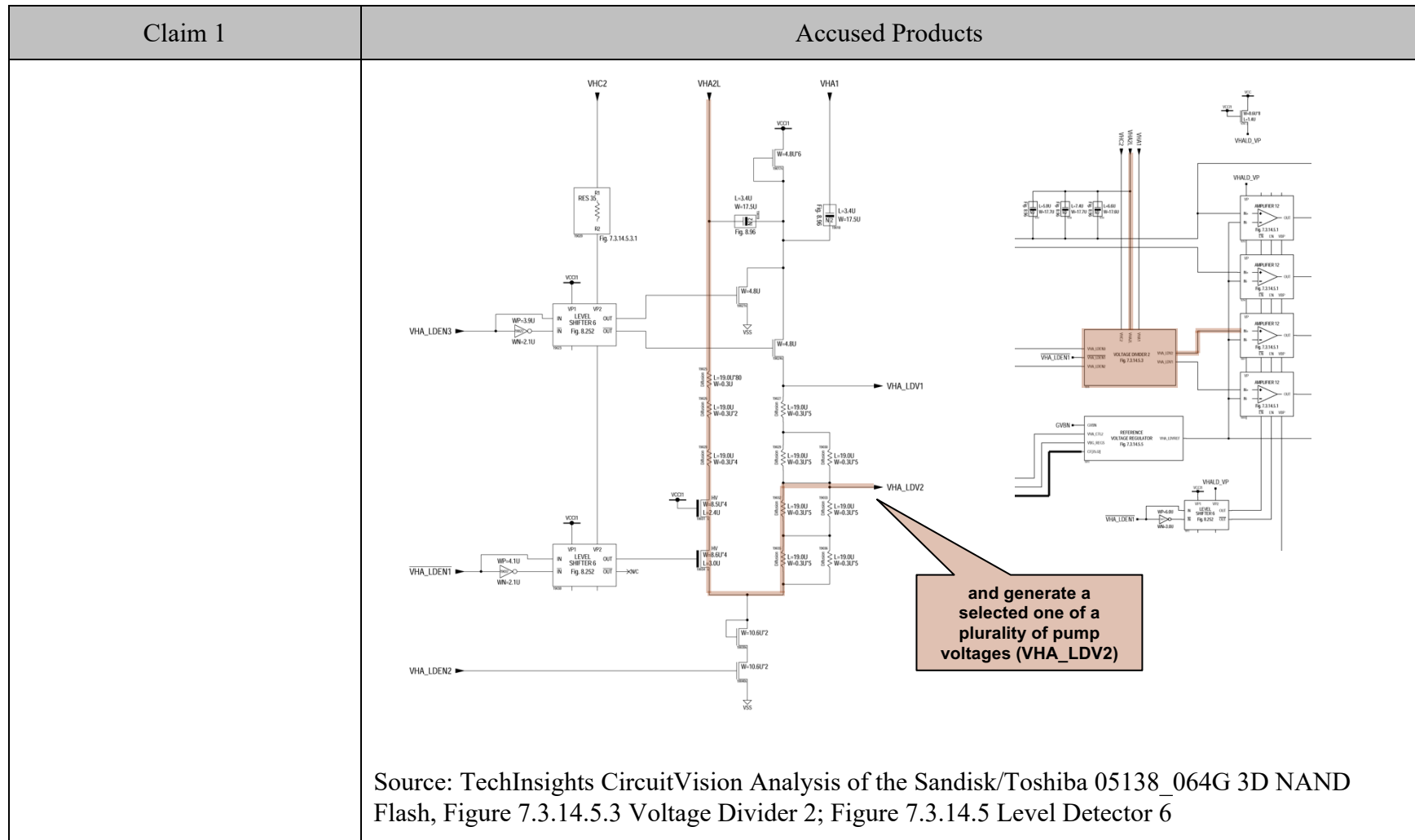
Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4

Claim 1	Accused Products
	 <p>The diagram shows a circuit for a voltage switch (VHA2). It includes an input (IN) and an output (OUT). The circuit features several MOSFETs and inductors. A callout box points to a specific MOSFET and inductor combination, stating: "and generate a selected one of a plurality of pump voltages (VHA2L)".</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.1 Voltage Switch 51</p>

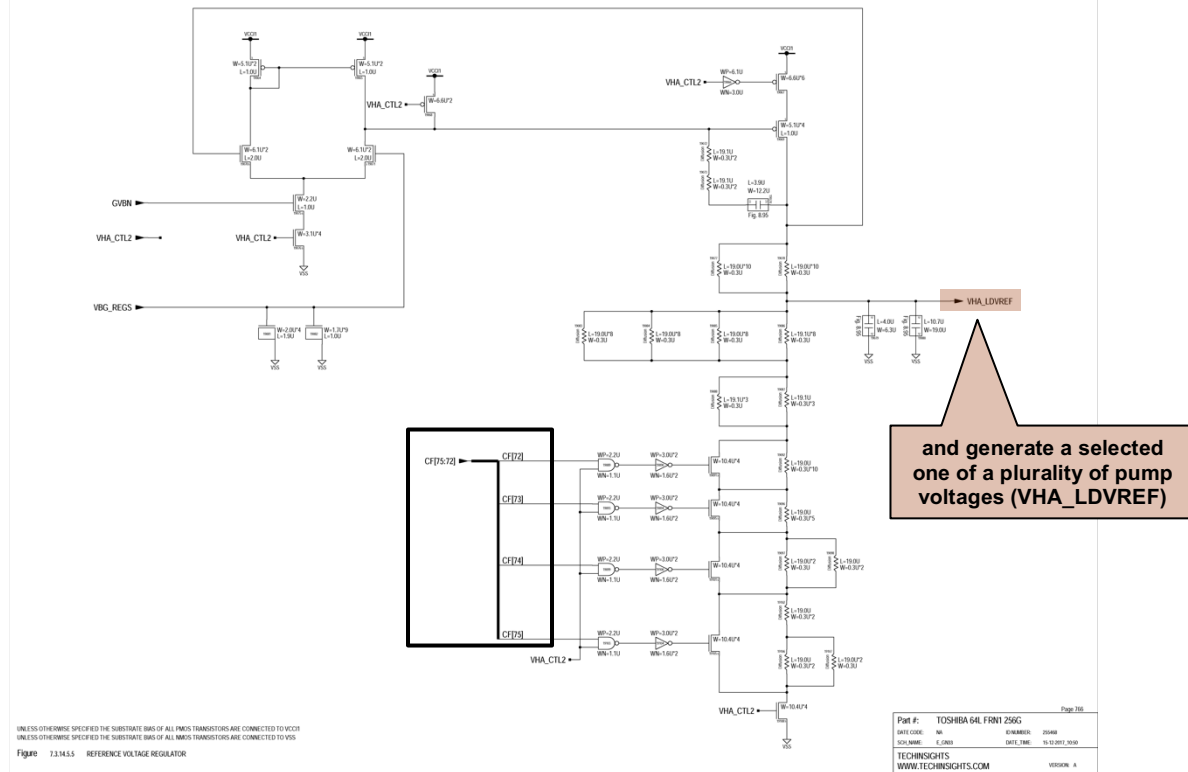
Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>



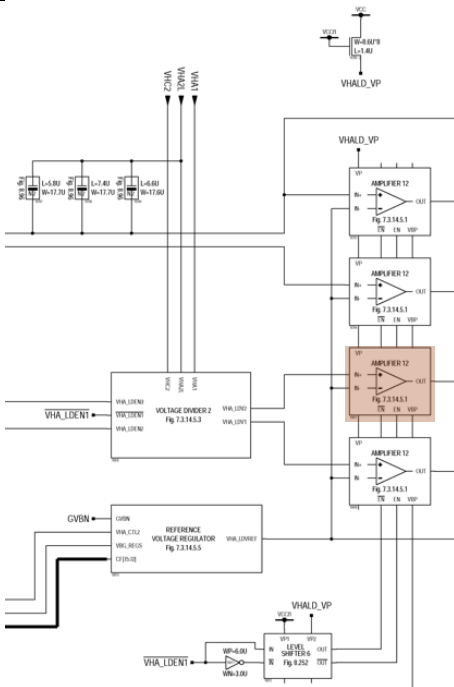
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Claim 1

Accused Products

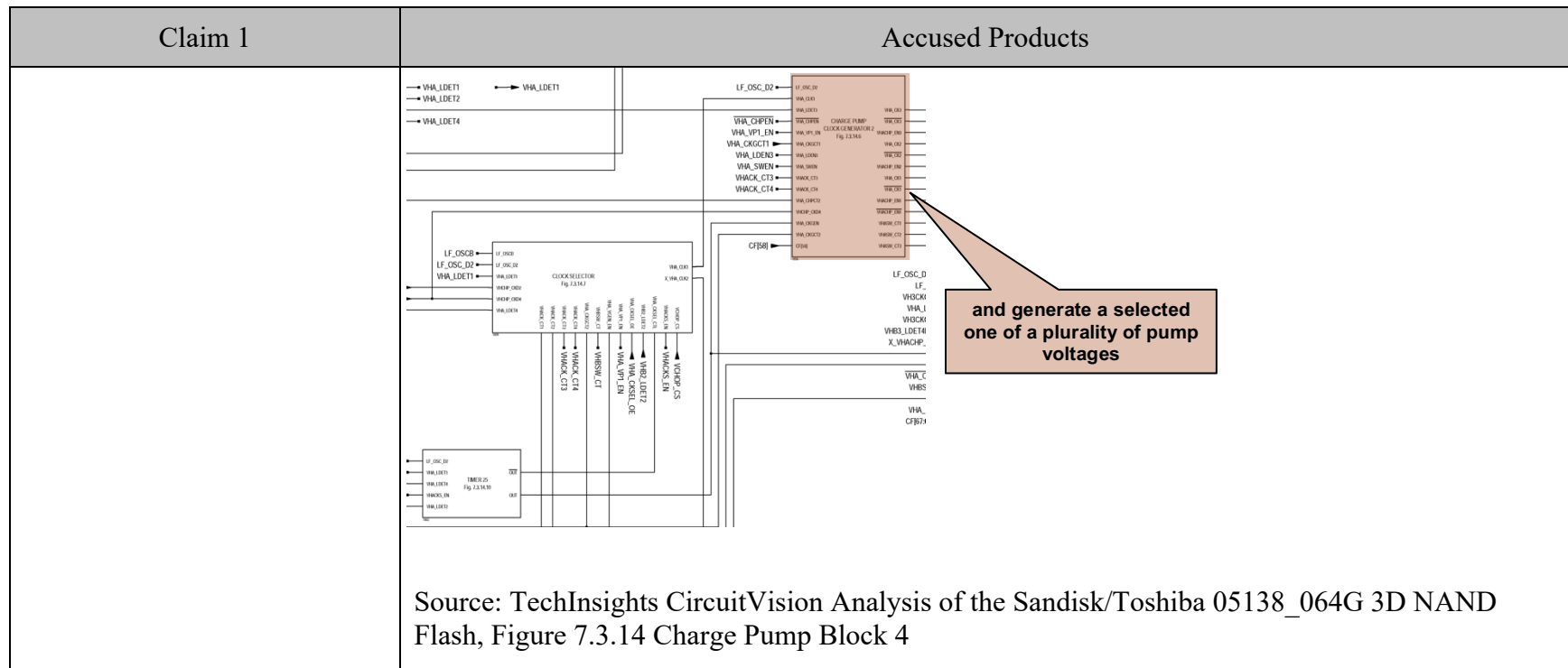


Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.5 Reference Voltage Regulator

Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

[illegible]

Claim 1	Accused Products
	<p>VHA_LDET3 = 1 Disables VHA_CK2 pump clock to 1 level</p> <p>VHA_CK2 = 1 VHA_CK2* = 0</p>



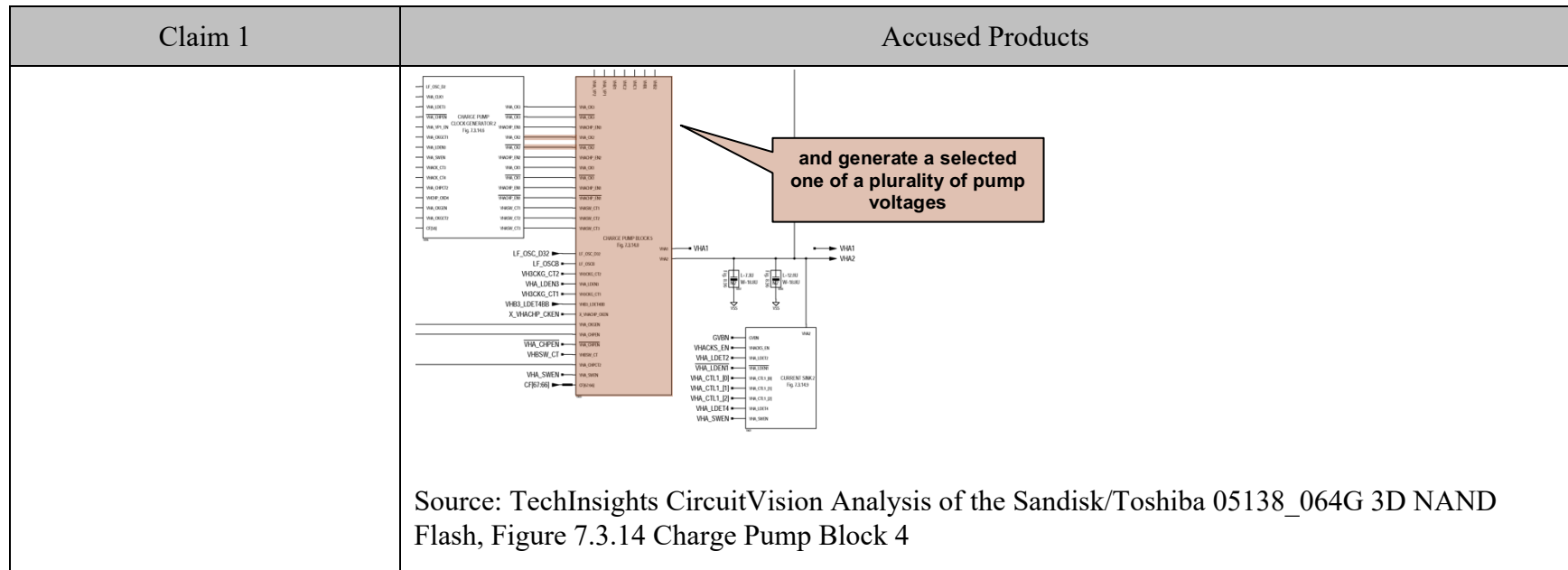
Claim 1

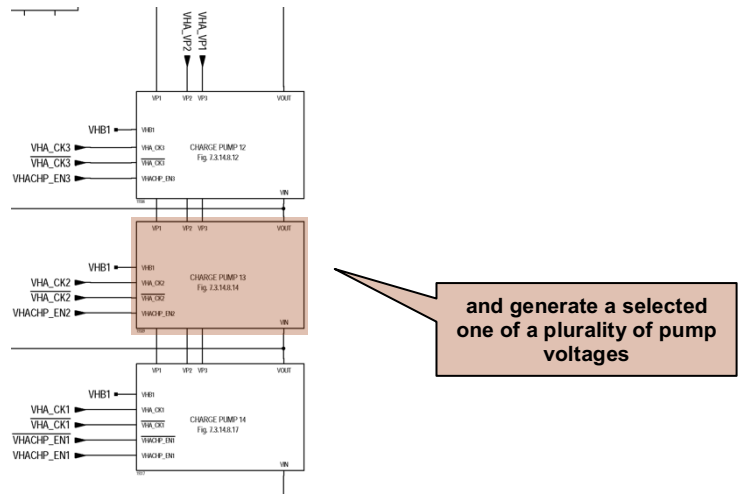
Accused Products

and generate a selected one of a plurality of pump voltages

a pumping circuit

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

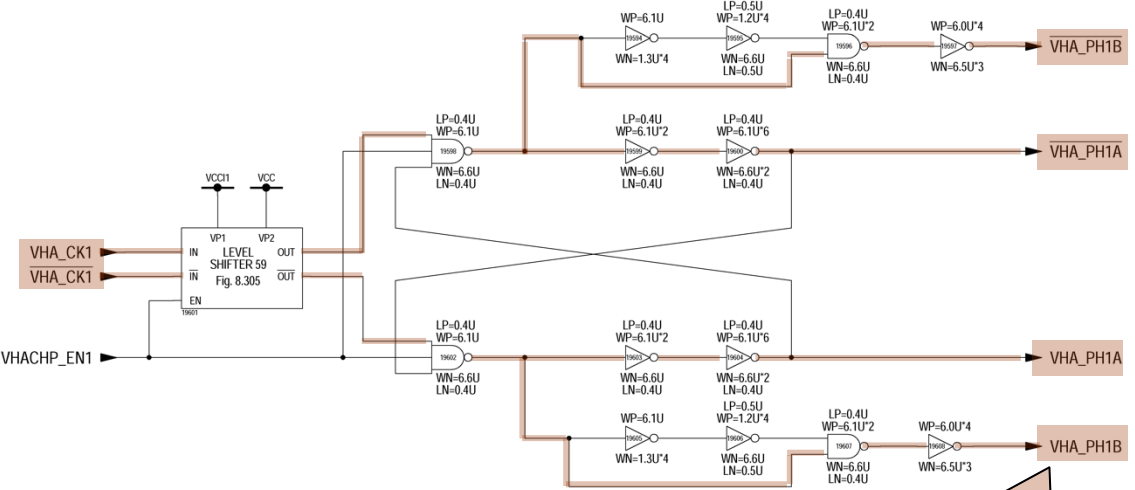


Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

Claim 1

Accused Products

and generate a selected one of a plurality of pump voltages

Claim 1	Accused Products
	<p data-bbox="638 354 758 415">VHA_CK2 VHA_CK2*</p> <p data-bbox="1633 293 1766 415">VHA_PH2A VHA_PH2A* VHA_PH2B VHA_PH2B*</p>  <p data-bbox="1556 954 1871 1003">and generate a selected one of a plurality of pump voltages</p> <p data-bbox="638 1052 1829 1122">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.12.6 Non-Overlapping Clock Generator 6</p>

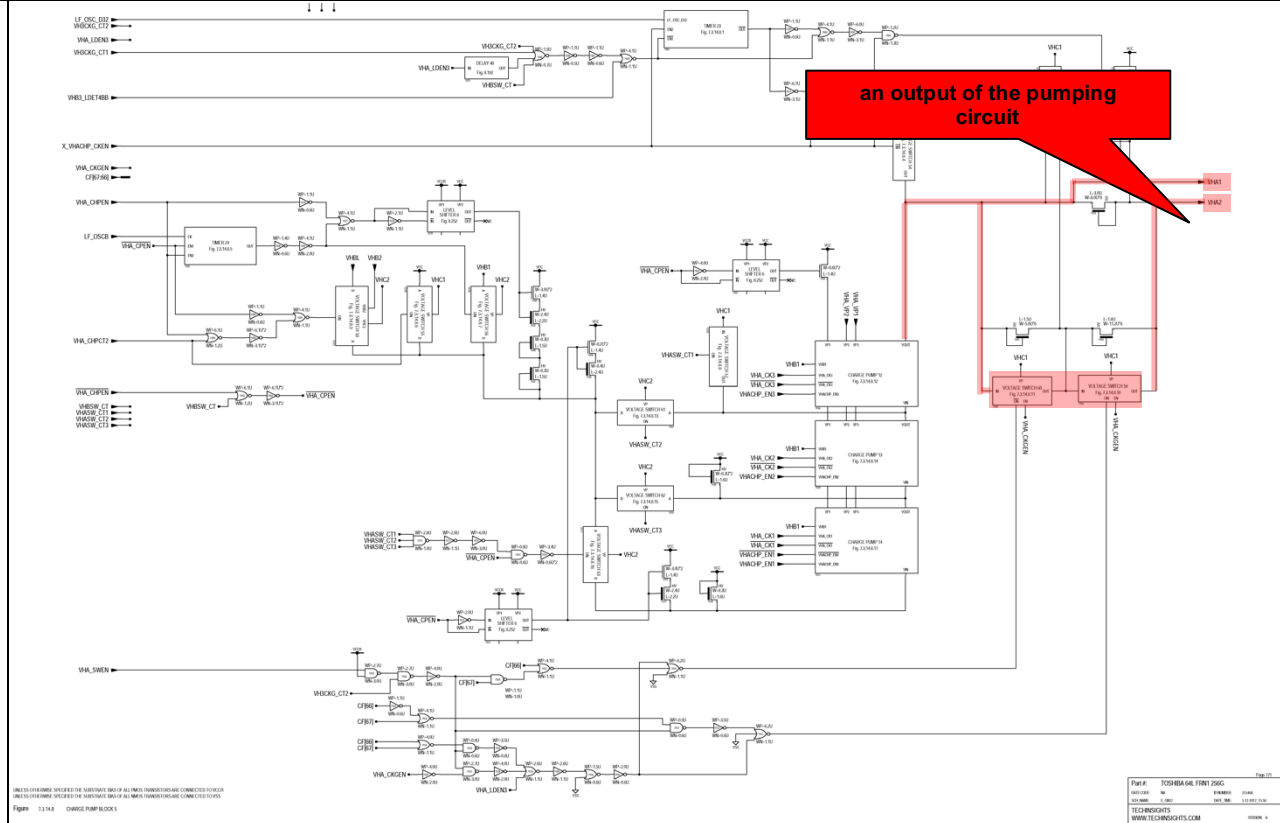
Claim 1	Accused Products

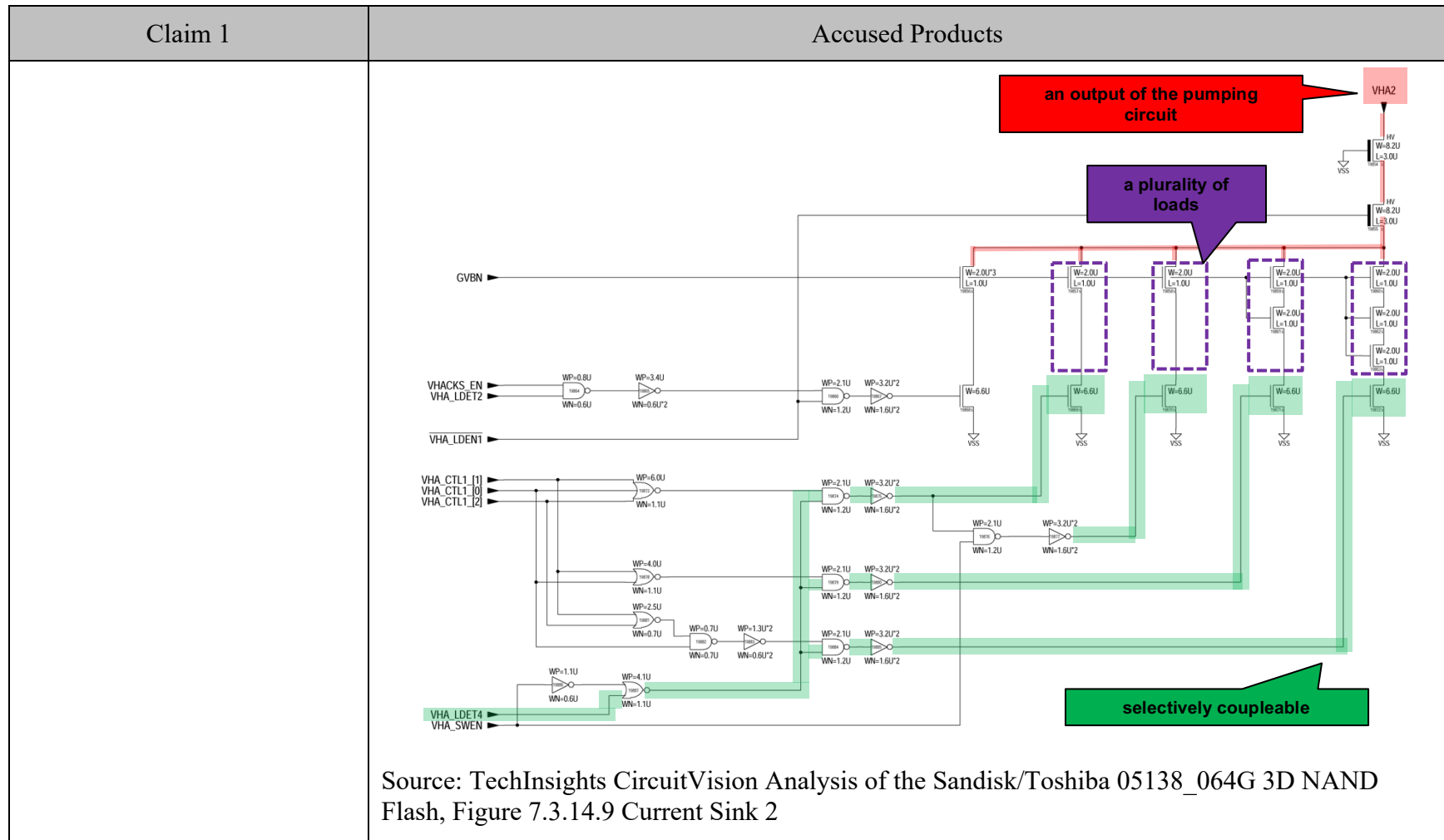
<p>Claim 1</p>	<p>Accused Products</p>
	<div data-bbox="1512 277 1873 440" style="border: 1px solid black; padding: 5px; margin-bottom: 10px;"> <p>and generate a selected one of a plurality of pump voltages</p> </div> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

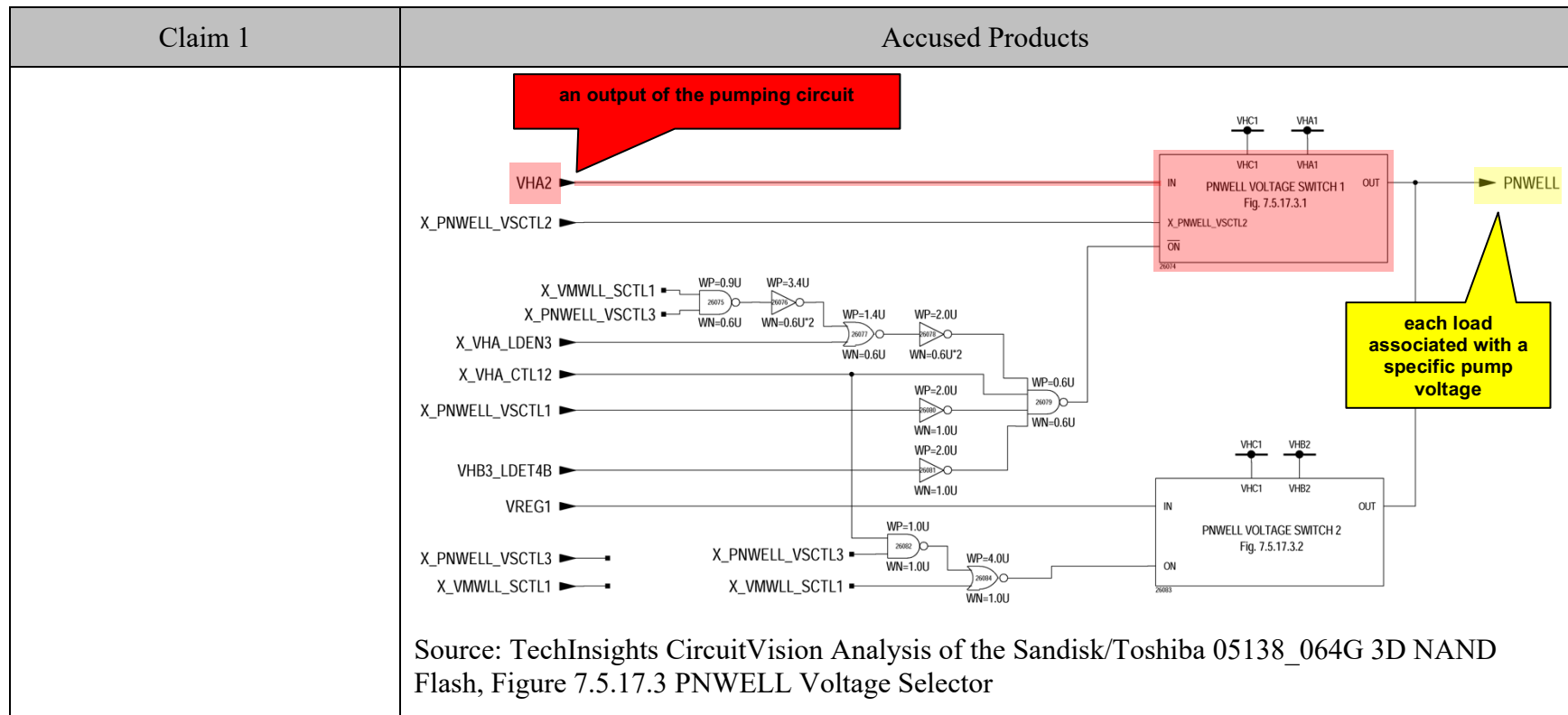
<p>Claim 1</p>	<p>Accused Products</p>
<p>[1b] b) a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage; and</p>	<p>Each Accused Product includes a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage.</p> <p>For example, VHA2 is an output of the pumping circuit of the Kioxia TSB3245. A plurality of loads (contained within Current Sink 2) can be selectively coupled to an output of the pumping circuit (for example VHA2). VHA2 is connected to pumping circuit output VHA1 through Voltage Switches 59 and 60. VHA1 is connected to wordline decoders during read or program operations. Read, program and erase operations require different voltages. Each load is associated with a specific pump voltage to carry out these functions.</p> <p>See, e.g.:</p>

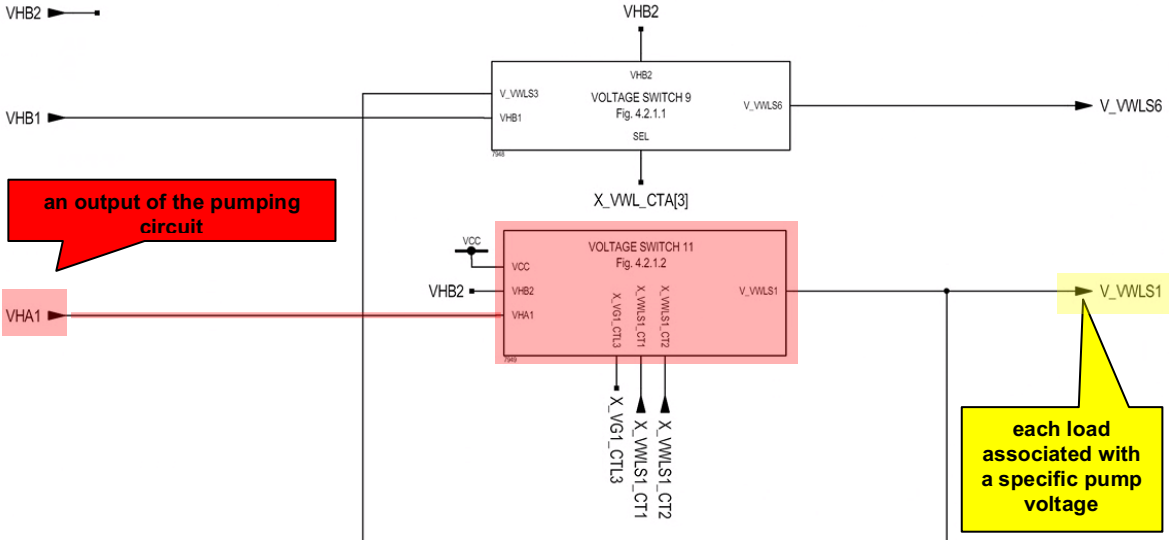
Claim 1

Accused Products

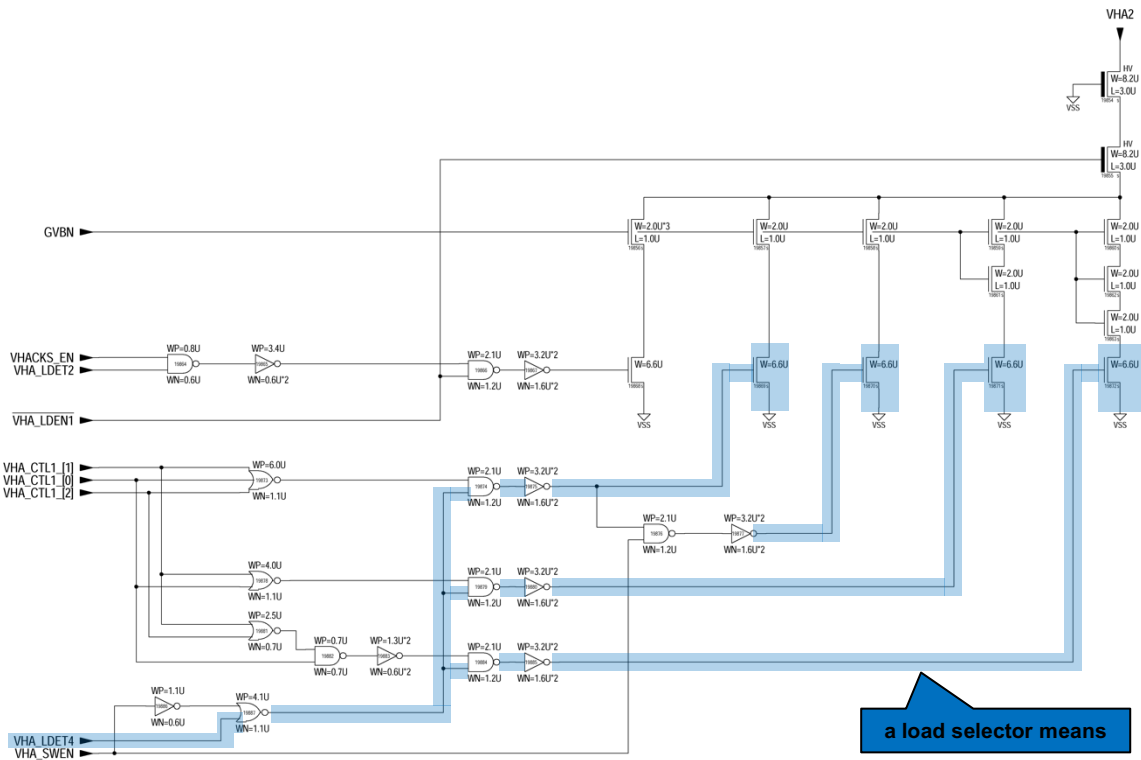


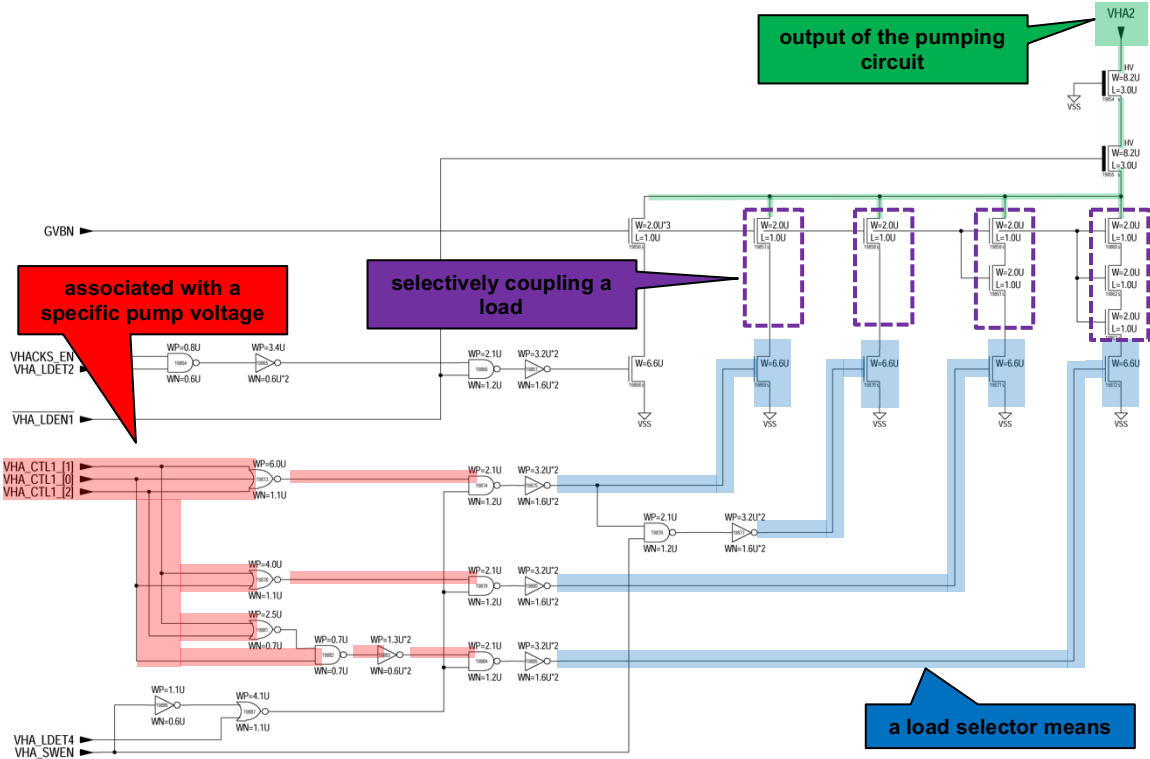




Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>[1c] c) a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p>	<p>Each Accused Product includes a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p> <p>For example, in the Kioxia TSB3245, the highlighted transistors below and their respective gate control signals form a load selector means. The output signal VHA_LDET4 from Level Detector 6 forms part of the load selector means. For example, the gate control signals are generated in part by a charge pump control signal (VHA_CTL1). This 3-bit value selectively couples a load associated with a specific pump voltage.</p> <p><i>See, e.g.:</i></p>

[illegible]

Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 1	Accused Products
	 <p>output of the pumping circuit</p> <p>associated with a specific pump voltage</p> <p>selectively coupling a load</p> <p>a load selector means</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 2

Claim 2	Accused Products
2. The charge pump circuit of claim 1, wherein the load selector means includes a	To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down

Claim 2	Accused Products
<p>target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p>	<p>the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p> <p>For example, in the Kioxia TSB3245, VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping.</p> <p><i>See evidence and explanation for claim element [1a], supra.</i></p>

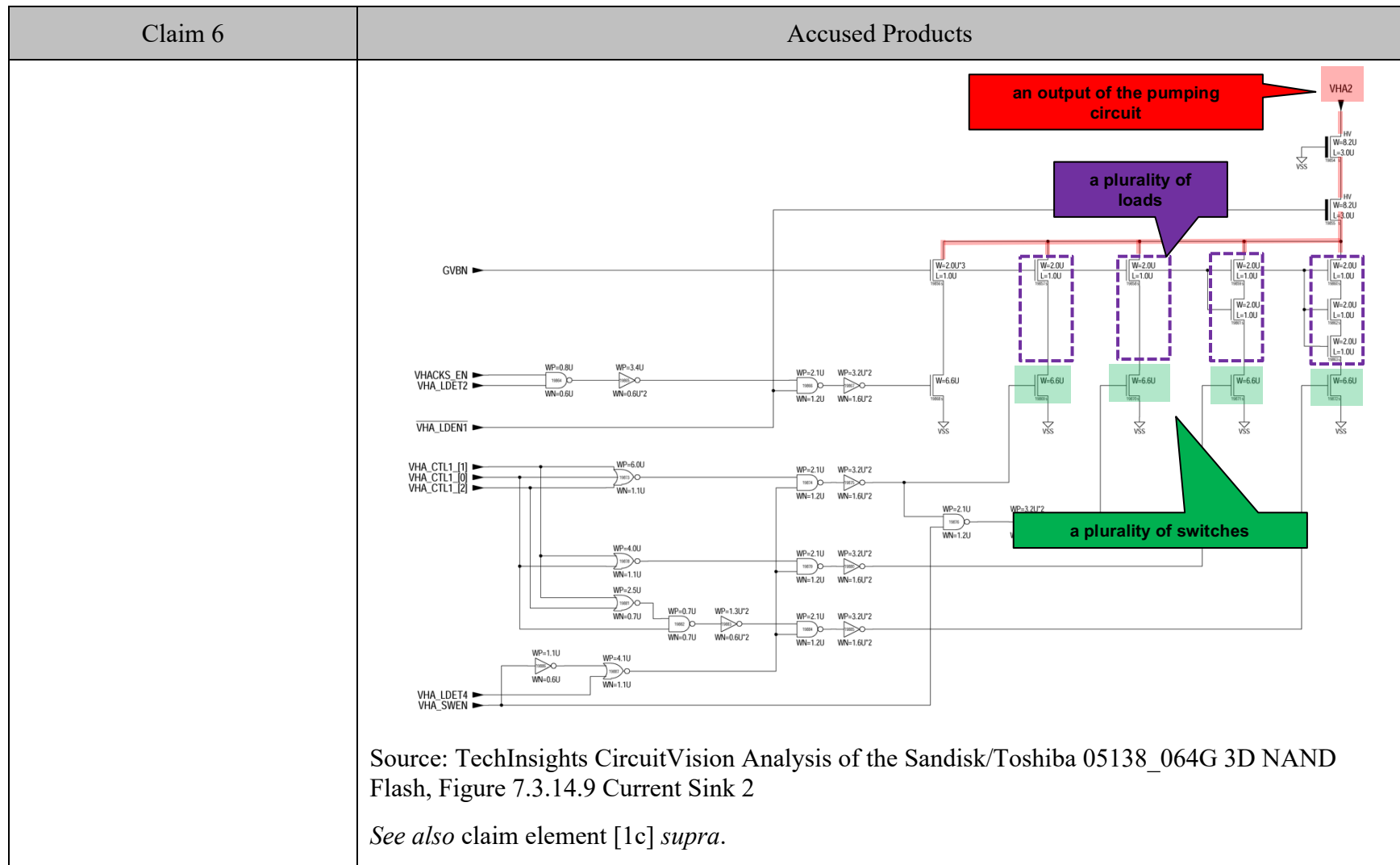
Claim 3

Claim 3	Accused Products
<p>3. The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, and whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref).</p> <p><i>See evidence and explanation for claim element [1a] and claim 2, supra.</i></p>

Claim 3	Accused Products
less than or equal to the reference voltage (V_{ref}).	

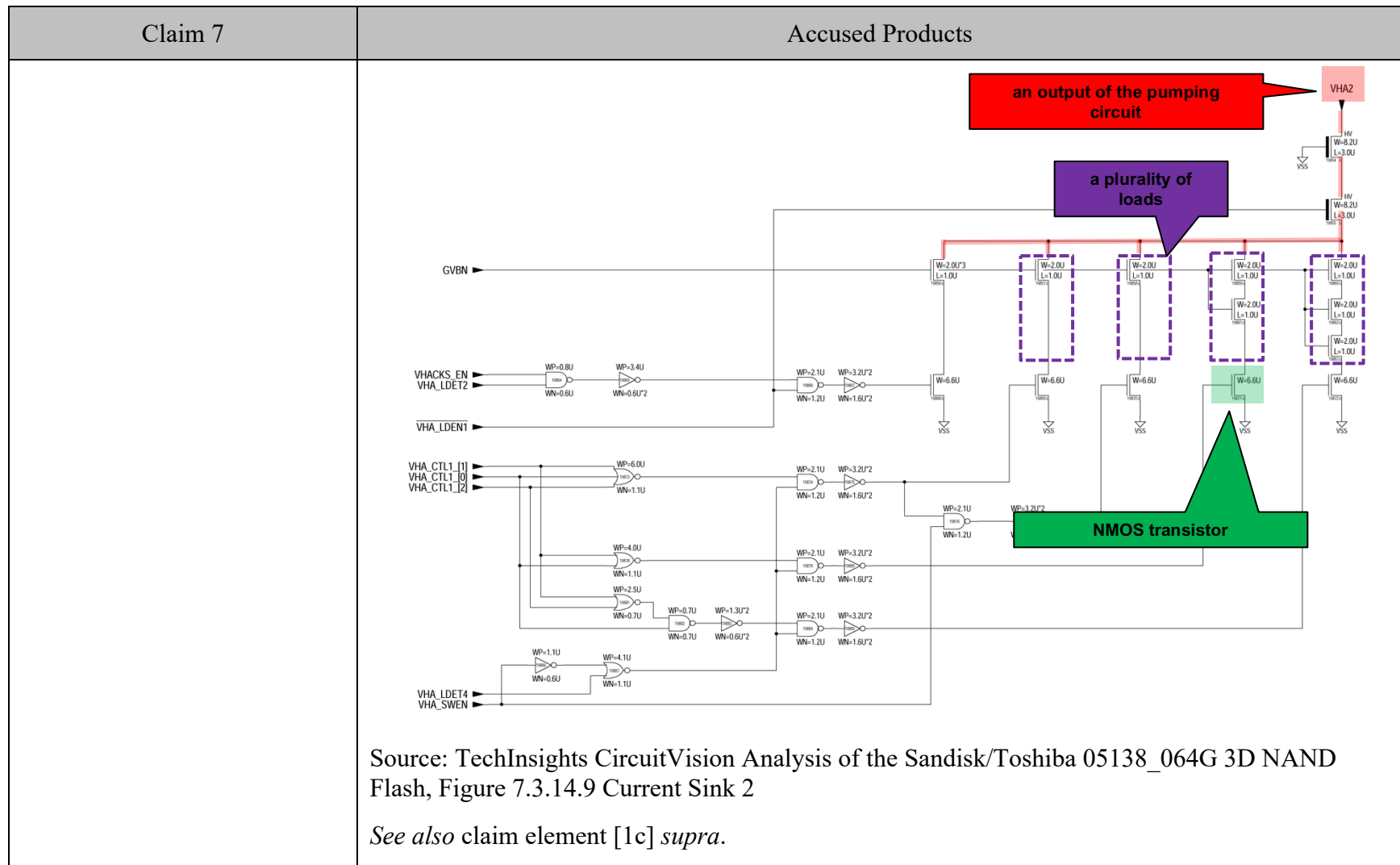
Claim 6

Claim 6	Accused Products
6. The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p> <p><i>See, e.g.:</i></p>



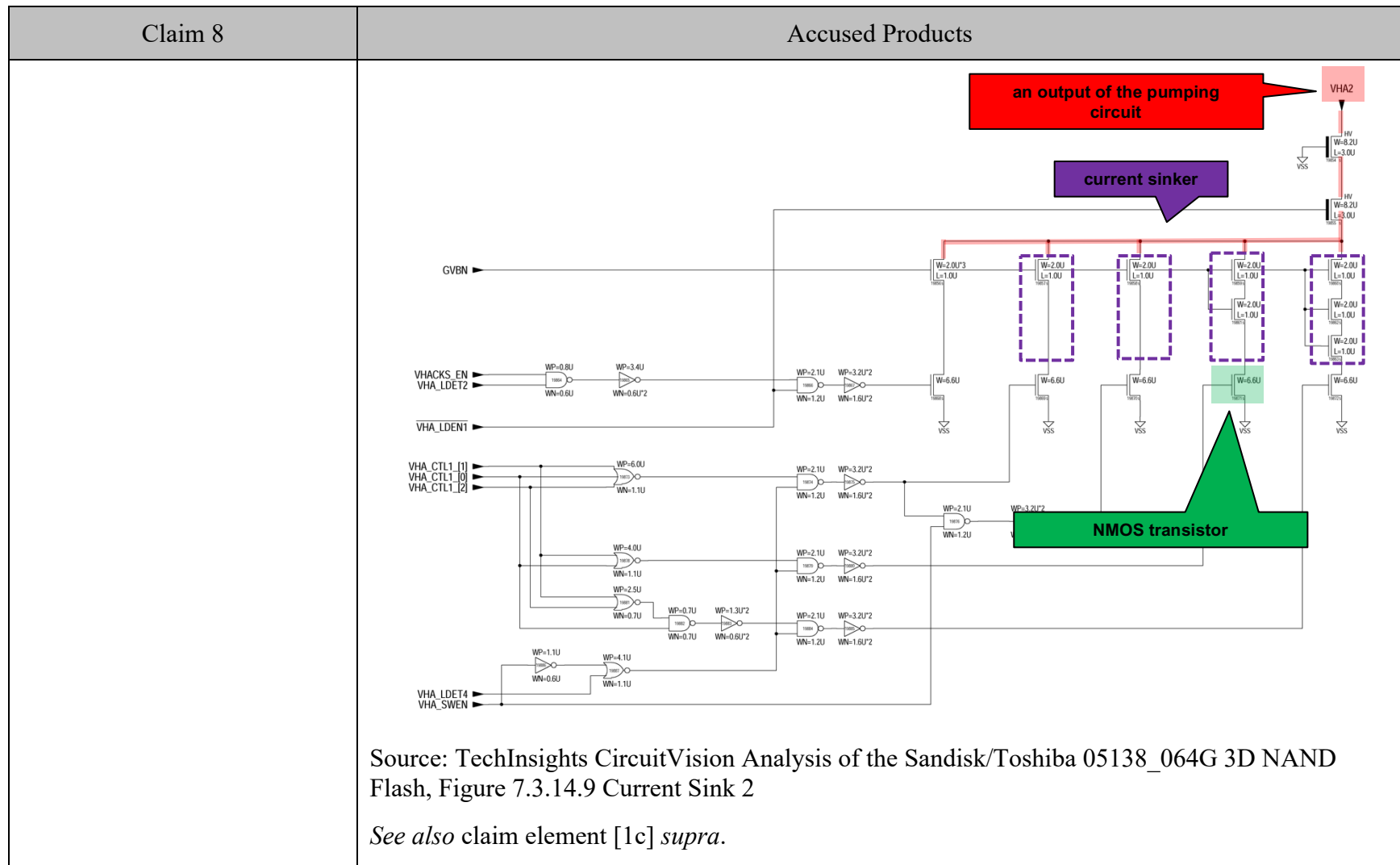
Claim 7

Claim 7	Accused Products
<p>7. The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p> <p><i>See, e.g.:</i></p>



Claim 8

Claim 8	Accused Products
<p>8. The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p> <p><i>See, e.g.:</i></p>

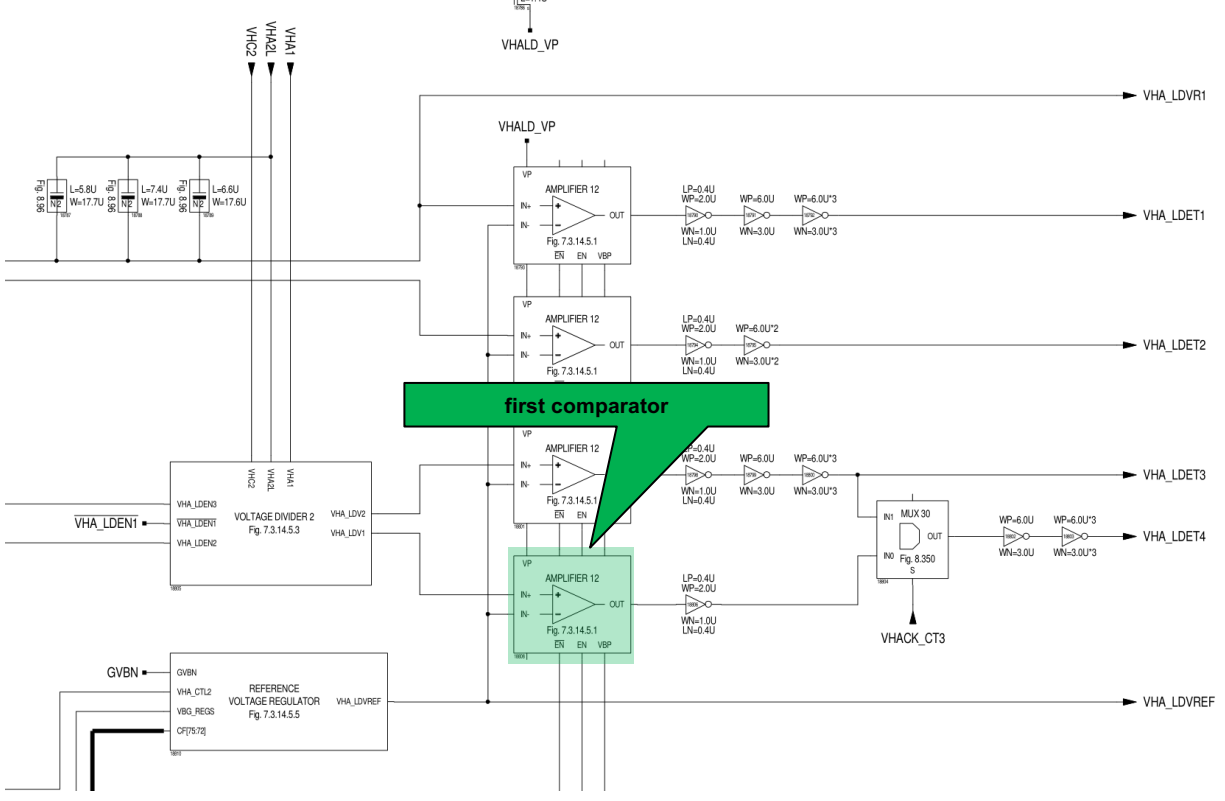


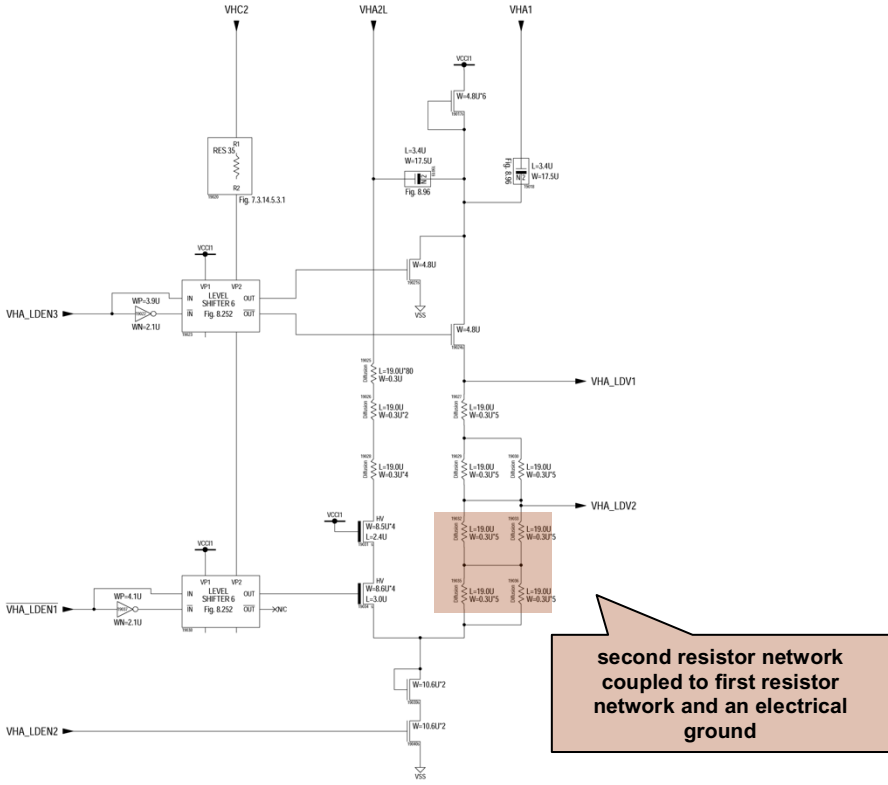
Claim 11

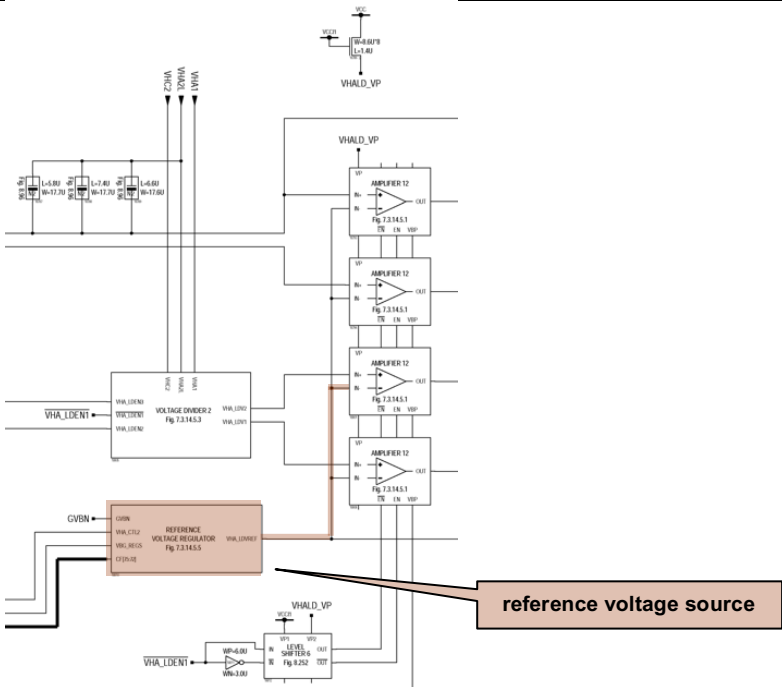
Claim 11	Accused Products
[11pre] 11. The charge pump circuit of claim 2 wherein the target output pump selector comprises:	Each Accused Product includes the charge pump circuit of claim 2. <i>See supra</i> claim 2.
[11a] a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref);	Each Accused Product includes a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref). <i>See, e.g.:</i>

Claim 11	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11b] b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator;</p>	<p>Each Accused Product includes a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11c] c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the</p>	<p>Each Accused Product includes a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
<p>second resistor network being coupled to an electrical ground; and</p>	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2</p>
<p>[11d] d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p>	<p>Each Accused Product includes a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p> <p>See, e.g.:</p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>